WHAT IS CLAIMED IS:

1. A method for reducing thermal dissipation in a single PLC package, said method comprising the steps of:

implementing a pulse width modulated (PWM) current regulator including a field effect transistor switch (FET), and

utilizing a turn on delay of the FET to provide a wide operating range of current.

2. A method according to Claim 1 wherein said step of implementing a PWM current regulator further comprises the step of implementing a PWM current regulator including a feed-back control loop.

3. A method according to Claim 1 further comprising the step of maintaining a relatively consistent noise to signal ratio down to an approximate near zero output level.

4. A method according to Claim 1 wherein said step of utilizing a turn on delay further comprises the step of utilizing a turn on delay of the FET to provide an operating range of current of greater than ten to one.

5. A method according to Claim 1 wherein said step of utilizing a turn on delay further comprises the step of utilizing a turn on delay of the FET to provide an operating range of current of greater than one hundred to one.

6. A method according to Claim 1 wherein said step of utilizing a turn on delay further comprises the step of utilizing a turn on delay of the FET to provide an operating range of current of greater than two hundred to one.

7. A method according to Claim 1 wherein said step of utilizing a turn on delay further comprises the step of reducing a duty cycle of the PWM.

8. A method according to Claim 1 further comprising utilizing the FET to dominate an inductive path of an output filter.

9. A method according to Claim 8 wherein said step of utilizing the FET further comprises the step of altering an impedance between a source of the FET

and a drain of the FET such that the impedance between the source and the drain dominates the inductive path of the output filter.

10. A method according to Claim 1 wherein said step of utilizing a turn on delay further comprises the steps of:

comparing a triangle wave reference signal to a command signal; and

reducing a duty cycle in response to said comparison.

11. A circuit for reducing thermal dissipation in a single PLC package, said circuit comprising:

a drive circuit comprising a field effect transistor (FET) including a drain and a gate;

an output circuit including a load terminal, said output circuit connected to said drain;

a feedback amplifier connected to said output circuit; and

an error amplifier circuit connected to said feedback amplifier and to said gate.

12. A circuit according to Claim 11 wherein said drive circuit further comprises a comparator comprising a first input, a second input, and an output, said output connected to said gate of said FET, said comparator configured to adjust a duty cycle of said FET in response to a command signal applied to said first input and a triangle wave applied to said second input.

13. A circuit according to Claim 11 wherein said drive circuit is configured to maintain a relatively consistent noise to signal ratio down to an approximate near zero output level at said load terminal.

14. A circuit according to Claim 11 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than ten to one.

15. A circuit according to Claim 11 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than one hundred to one.

16. A circuit according to Claim 11 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than two hundred to one.

17. A circuit according to Claim 11 further comprising a timing circuit configured to provide a triangle wave to said drive circuit.

18. A circuit according to Claim 17 wherein said timing circuit comprises a monolithic timing circuit.

19. A circuit according to Claim 11 wherein said drive circuit is configured to:

compare a triangle wave reference signal to a command signal; and

adjust a duty cycle in response to said comparison.

20. A PLC comprising:

a CPU;

a bus interface operationally coupled to said CPU;

at least one memory unit operationally coupled to said bus interface;

at least one I/O module operationally coupled to said bus interface; and

a current regulator operationally coupled to said I/O module, said current regulator comprising:

a drive circuit comprising a field effect transistor (FET) including a drain and a gate;

an output circuit including a load terminal, said output circuit connected to said drain;

a feedback amplifier connected to said output circuit; and

an error amplifier circuit connected to said feedback amplifier and to said gate.

21. A PLC according to Claim 20 wherein said drive circuit further comprises a comparator comprising a first input, a second input, and an output, said output connected to said gate of said FET, said comparator configured to reduce a duty cycle of said FET in response to a command signal applied to said first input and a triangle wave applied to said second input.

22. A PLC according to Claim 20 wherein said drive circuit is configured to maintain a relatively consistent noise to signal ratio down to an approximate near zero output level at said load terminal.

23. A PLC according to Claim 20 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than ten to one.

24. A PLC according to Claim 20 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than one hundred to one.

25. A PLC according to Claim 20 wherein said drive circuit is configured to utilize a turn on delay of the FET to provide an operating range of current of greater than two hundred to one.

26. A PLC according to Claim 20 wherein said current regulator further comprises a timing circuit configured to provide a triangle wave to said drive circuit.

27. A PLC according to Claim 26 wherein said timing circuit comprises a monolithic timing circuit.

28. A PLC according to Claim 20 wherein said drive circuit is configured to:

compare a triangle wave reference signal to a command signal; and

adjust a duty cycle in response to said comparison.